What is claimed is:

1. A circuit for successive approximation analog-to-digital conversion, comprising:

a noise-compensating comparator circuit that is configured to provide a comparator output signal in response to a first comparison signal, a second comparison signal, a first reference signal, and a second reference signal,

wherein the noise-compensating comparator circuit is configured to combine the first comparison signal, the second comparison signal, the first reference signal, and the first second reference signal to provide a differential signal such that a noise component of the first comparison signal is substantially cancelled out;

a successive approximation logic circuit that is configured to provide a digital output signal from the comparator output signal; and

a digital-to-analog converter circuit that is configured to provide the first comparison signal from the digital output signal.

2. The circuit of Claim 1, wherein the noise-compensating comparator circuit is configured to combine a signal derived from the first comparison signal with a signal derived from the second reference signal to provide a first half of the differential signal, and further configured to combine a signal derived from the second comparison signal with a signal derived from first reference signal such that the noise component of the first comparison signal is substantially cancelled out differentially.

3. The circuit of Claim 1, wherein the noise-compensating comparator circuit includes:

a first differential pair, wherein the first differential pair includes a first transistor and a second transistor;

a second differential pair, wherein the second differential pair having a third transistor and a fourth transistor, a drain of the third transistor is coupled to a drain of the second transistor, a drain of the fourth transistor is coupled to a drain of the first

transistor, and wherein the first and second differential pairs are configured to provide a differential current; and

a comparator that is configured to provide the comparator output signal from the differential current.

4. The circuit of Claim 1, wherein the digital-to-analog converter circuit is a multiplying digital-to-analog converter circuit.

5. The circuit of Claim 1, further comprising:

a first reference circuit that is configured to provide the first reference signal such that the first reference signal includes a first DC component and a noise component superimposed on the first DC component, wherein the noise component of the first reference signal is substantially similar to the noise component of the first comparison signal; and

a second reference circuit that is configured to provide the second reference signal such that the second reference signal includes a second DC component, wherein the second DC component is substantially similar to the first DC component.

6. The circuit of Claim 5, wherein the first reference circuit includes:

a current source circuit that is configured to provide a current; and

a resistor that is configured to provide the first DC component in response to the current.

7. The circuit of Claim 5, wherein the first reference circuit includes:

a reference voltage circuit that is configured to provide the first DC component; and

a replicating circuit that is configured to provide the noise component of the first reference signal.

8. The circuit of Claim 7, wherein the replicating circuit includes a substantial replica of at least a portion of the digital-to-analog converter circuit.

9. The circuit of Claim 7, wherein the replicating circuit includes:

a plurality of capacitors; and

a plurality of switches, wherein the plurality of switches are coupled to the plurality of capacitors.

10. The circuit of Claim 9, wherein the digital-to-analog converter circuit includes a voltage divider configured to provide the first comparison signal according to a resistance ratio of the voltage divider, and

wherein the successive approximation logic circuit is configured to control the switching of the plurality of capacitors such that an impedance ratio of the plurality of capacitors is substantially similar to the resistance ratio of the voltage divider.

11. The circuit of Claim 9, wherein the plurality of capacitors is similar to capacitors of the digital-to-analog converter circuit, and wherein the plurality of switches is adapted to operate substantially similarly to how switches of the digital-to-analog converter circuit are adapted to operate.

12. The circuit of Claim 11, wherein the switches of the digital-to-analog converter are configured to open and close responsive to a number of bits of the digital output signal.

13. A method for successive approximation analog-to-digital conversion, comprising:

combining a first comparison signal, a second comparison signal, a first reference signal, and a first second reference signal to provide a differential signal;

comparing a first half and a second half of the differential signal to provide a comparison result signal;

employing successive approximation logic to provide a digital output signal from the comparison result signal; and

employing digital-to-analog conversion to provide the first comparison signal from the digital output signal.

14. The method of Claim 13, wherein combining includes:

providing a differential current such that a first half of the differential current corresponds to a sum of a current associated with a signal derived from the first comparison signal and a current associated with a signal derived from the second reference signal, and such that a second half of the differential current corresponds to a sum of a current associated with a signal derived from the second comparison signal and a current associated with a signal derived from the first reference signal,

wherein the differential signal is derived from the differential current.

15. The method of Claim 13, wherein the digital-to-analog conversion is a multiplying analog-to-digital conversion.

16. The method of Claim 13, wherein combining is accomplished such that a noise component of the first comparison signal is substantially cancelled out.

17. The method of Claim 13, further comprising:

generating the first reference signal such that the first reference signal includes a noise component that is substantially similar to a noise component of the first comparison signal.

18. The method of Claim 17, wherein the first reference signal is generated such that the first reference signal further includes a DC reference component.

19. The method of Claim 17, further comprising:

generating the second reference signal such that the second reference signal includes a DC reference level wherein the first reference signal is generated such that the first reference signal further includes a DC reference component that is substantially similar to the DC reference component.

20. A circuit for successive approximation analog-to-digital conversion, comprising:

means for combining a first comparison signal, a second comparison signal, a first reference signal, and a first second reference signal to provide a differential signal;

means for comparing a first half and a second half of the differential signal to provide a comparison result signal;

means for employing successive approximation logic to provide a digital output signal from the comparison result signal; and

means for employing digital-to-analog conversion to provide the first comparison signal from the digital output signal.